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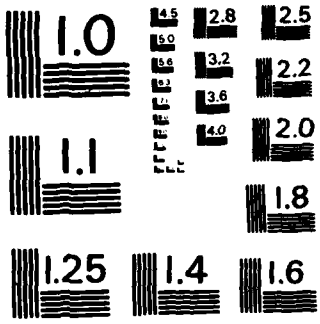

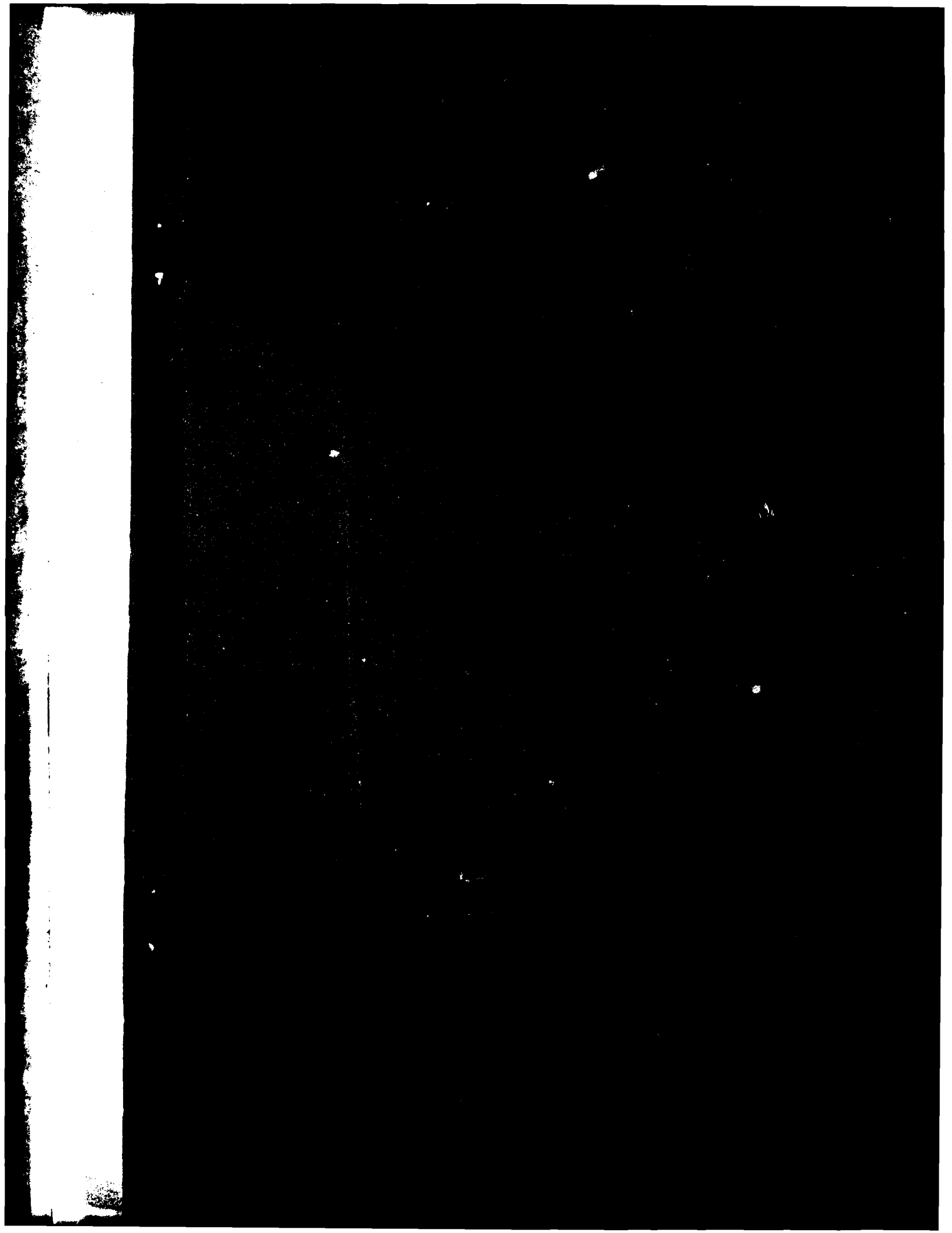

ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3583

TITLE: AN INTRODUCTION TO THE AXIS TEST BOX

AUTHOR: A L Simcock

DATE: April 1983

SUMMARY

This Memorandum describes, briefly, Project AXIS and why a Test Box is needed. The role of the Test Box within the AXIS Project is also described. This document also acts as a guide to the AXIS Test Box documentation.

RSRE MEMORANDUM NO 3583

AN INTRODUCTION TO THE AXIS TEST BOX

A L Simcock

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LIST OF ABBREVIATIONS

GTU GROUP TERMINATING UNIT
TDM TIME DIVISION MULTIPLEXED
CPU CENTRAL PROCESSOR UNIT
SIU SERIAL INTERFACE UNIT
SUT SYSTEM UNDER TEST
FSA FRAME SYNCHRONISATION AND ALIGNMENT
CDU CODE DETECTOR UNIT
TSU TRUNK SIGNALLING UNIT
VDU VISUAL DISPLAY UNIT
RAM RANDOM ACCESS MEMORY
ROM READ ONLY MEMORY
PPI PROGRAMMABLE PERIPHERAL INTERFACE
AXIS AUTOMATIC EXCHANGE FOR THE INVESTIGATION OF STRUCTURED SOFTWARE

Ø THE Ø SYMBOL IS USED TO REPRESENT ZERO IN ORDER THAT IT MAY EASILY BE DISTINGUISHED FROM THE LETTER O.

1 INTRODUCTION

This memorandum provides an introduction to the AXIS Test Box, and briefly describes project AXIS and the role of the Test Box in the AXIS research programme. This report is the first in a series of four reports describing the AXIS Test Box. The second report (ref 1) is the Operating Guide, the third (ref 2) is the Software report and the fourth (ref 3) the Hardware report.

2 PROJECT AXIS

The AXIS switch (Fig 1) consists of a central processor which controls a switching matrix and a number of group terminating units (GTU). Each GTU serves a line carrying a traffic group, which is a set of subscriber channels multiplexed together, derived either from a local multiplexer or over a trunk link connected to another switch. The channels are digital, operating at 16kb/s, and 16 or 32 are time-division multiplexed together. The switching Matrix is able to connect together individual subscriber channels from the same or different groups. One channel in each group is reserved for TDM framing, and another, in trunk groups, to carry trunk signalling messages. Both GTU and Matrix present the same type of electrical interface to the controlling CPU, which is a Plessey System 25Ø.

The component parts of a GTU (Fig 2) differ somewhat depending on whether the GTU is serving a local or trunk group. Figure 2 illustrates the local role. In either case, the control interface to the CPU is accessed via a serial interface unit. Three types of information pass through the SIU:

i) commands to a command register which controls the other elements

ii) status from a status register which monitors these elements

iii) signalling information from a code detector unit which extracts inband signals generated by the subscribers (or, in the trunk serving role, to and from a trunk signalling unit).

The switching matrix (Figure 3) has a similar structure.

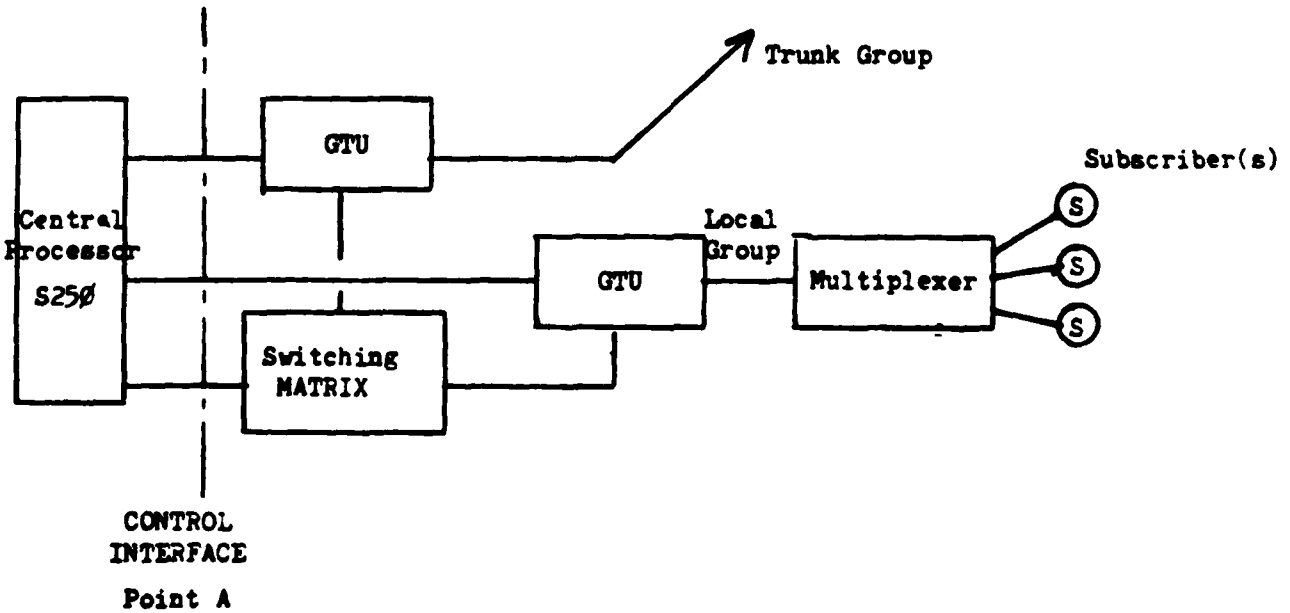

Fig. 1 AXIS SWITCH

3 AXIS TEST BOX

It is convenient to be able to develop and test the individual peripheral components of AXIS (GTUs, Matrix) in isolation. The Test Box offers a single interface identical to the control interface of the CPU, and permits its user to inject signals into a peripheral and monitors its responses freely. While programs exist which can be run in the CPU to fulfil the same purpose, they require familiarity with the rather complex operating system of the S 25Ø, and prevent its use as part of an operational switch while they are running.

A test box has been built entirely in hardware, but was found to have operational limitations; and therefore the microprocessor controlled Test Box was developed.

4 CONTROL INTERFACE DEFINITION

The interface between the GTU or Matrix and the System 25Ø (Point A in fig 1) takes the form of six pairs of balanced lines. Table 1 identifies these lines.

Name	Meaning	Direction
AX	Activity X	CPU ⟶ System under Test
DX	Data X	CPU ⟶ System under Test
TX	Timing X	CPU ⟶ System under Test
AY	Activity Y	System under Test ⟶ CPU
DY	Data Y	System under Test ⟶ CPU
TY	Timing Y	System under Test ⟶ CPU

Table 1 Plessey Interface

The inter-relationship of these signals is detailed in ref. 6. Point A in figure 1 is the position which the Test Box is used in the AXIS system, ie to replace the System 25Ø at this interface.

5 CONTROL OF THE SYSTEM UNDER TEST

The AXIS Test Box controls the System Under Test (SUT) via the interface described in Section 3. The interface point in each system, whether it is a Matrix or a GTU, is the Serial Interface Unit (SIU).

5.1 Control of the Matrix (See Fig. 3 and Ref 7).

Figure 3 illustrates the Matrix internal register structure. Outputs from the Test Box are sent to the Command or Connection Registers. Inputs are received from the Status and Connection Memory Registers. The Command Register is used to control the state of the circuits within the Matrix (ie to provide Reset etc). The Status Register monitors the responses to the commands.

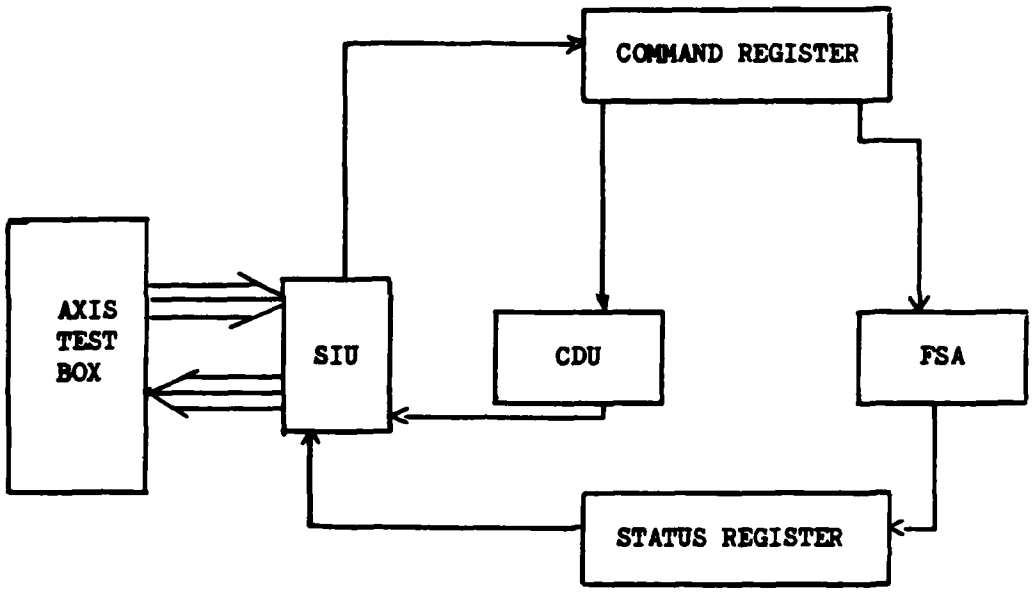

Fig 2. Block Diagram showing Registers Used in the GTU. When in Local Mode

N.B. When in Trunk Mode the CDU is replaced by a TSU.

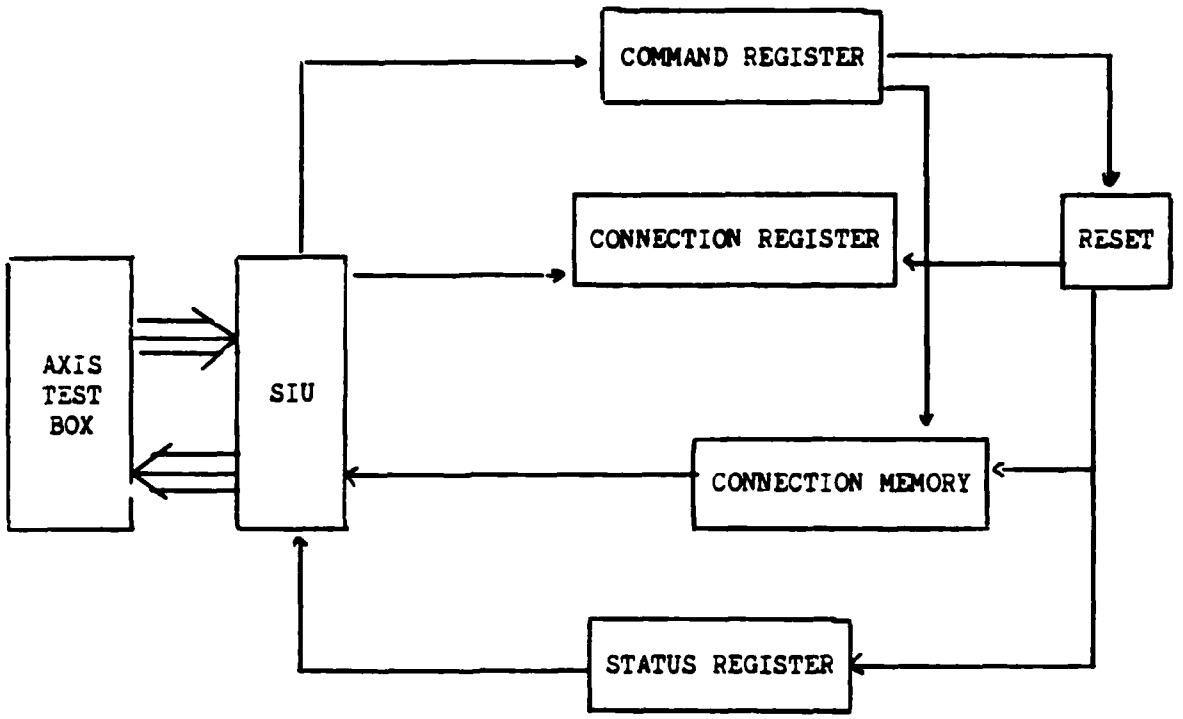

Fig 3 Block Diagram showing Registers used in the Matrix

Outputs to the Connection Register instruct the Matrix to make subscriber interconnections, and the Connection Memory keeps a record of the inter-connection information.

For a full description of these functions see Ref 7.

5.2 Control of the GTU (see Fig 2 and Ref 5)

Figure 2 illustrates the GTU internal register structure. Outputs from the Test Box are sent to the Command or Trunk Signalling Unit (TSU) register and inputs received from the Status, Code Detector (CDU) or TSU register. The command register is used to control the state of the circuit functions within the GTU, eg to instruct a Frame Sync search. Outputs to the TSU are sent by the TSU to other switches within the network (ie CPU to CPU information exchange).

Inputs from the Status register report the status of the internal GTU circuits. Inputs from the CDU contain the subscriber dialling information and TSU inputs contain information received from other CPUs in the network. For a full description of the internal structure of the GTU see Ref 5.

6 PHYSICAL DESCRIPTION OF THE AXIS TEST BOX

The AXIS Test Box has been built to be a transportable, self contained test facility. (See photograph Fig 4). It has been incorporated into a 19 inch rack system on wheels and includes its own power supplies, VDU for user interface to the Test Box, an oscilloscope and the Test Box itself. The actual Test Box occupies a single 19 inch rack (see Fig 5) and includes:-

a) The M68Ø9 microprocessor card.
b) Random Access Memory (RAM)
c) Read Only Memory (ROM)
d) Programmable Peripheral Interface (PPI) Devices
e) Dedicated Interface Hardware.

7 THE 'TWO CARD' SYSTEM

The AXIS Test Box employs a 'two card' system for producing output and input commands (shown in figure 5). That is, it uses one PPI card to control the Output Buffer Board for output commands and the other PPI card to control the Input Buffer Board for input commands. This makes the software easier to interpret, as specific memory addresses corresponding to PPI locations can now be recognised as input or output ports. Another design feature of the Test Box is that only some of the facilities available on the PPI are used (thus allowing future enhancement). Each PPI card carries two PPI chips, each chip has three ports, A, B and C, but only ports A and B are used on the PPI's employed in the AXIS Test Box as this serves to simplify the PPI programming, and allows for enhancements. For a full description of the Test Box Hardware see Ref 3.

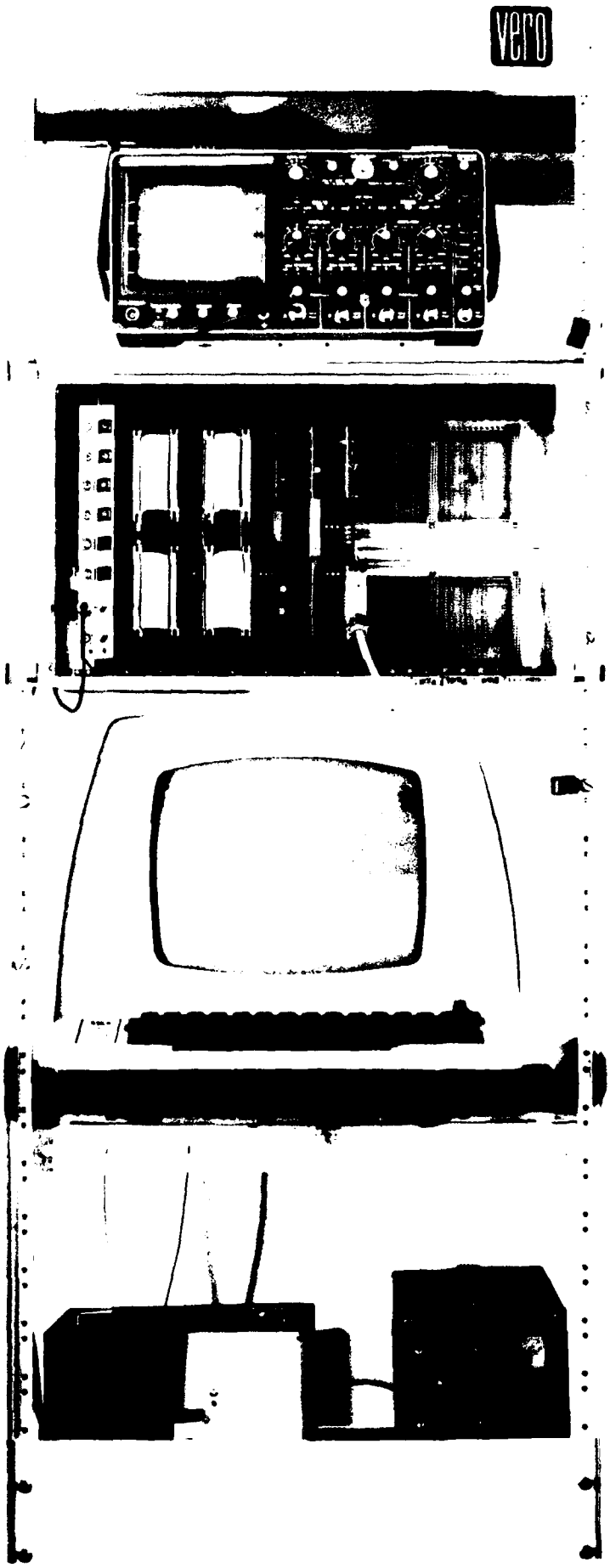

Fig 4
AXIS Test Box in Rack

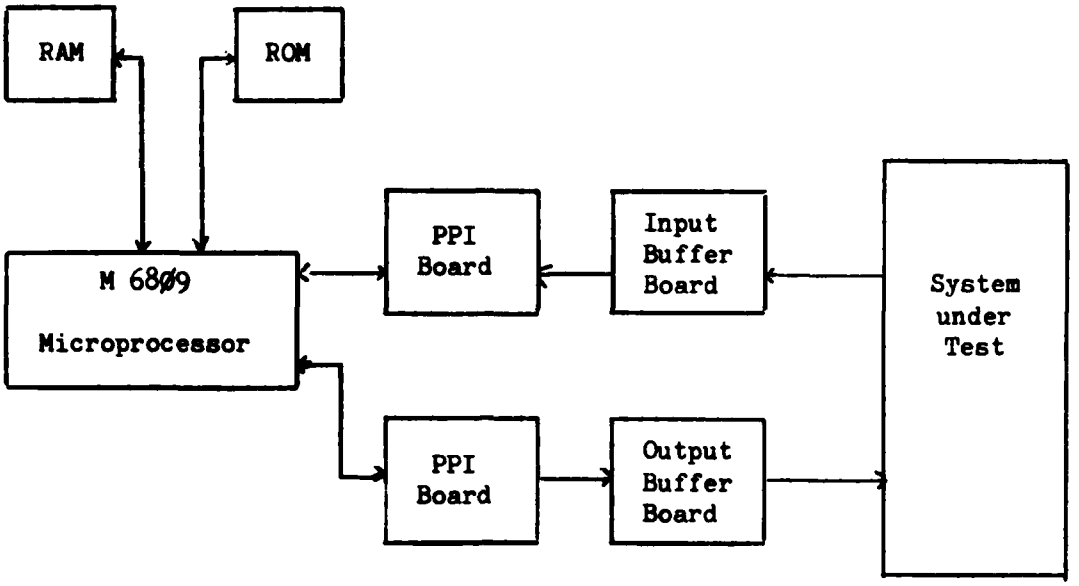

Fig 5 Block diagram of AXIS Test Box Illustrating the 'two card system'

8 CONCLUSIONS

The AXIS Test Box has already been extensively used, even by staff who had been reluctant to become involved with the complexity of testing using the System 25Ø.

Application hardware faults which had been difficult to isolate using the System 25Ø have been corrected by testing with the AXIS Test Box.

As the users become more familiar with the Test Box enhancements or improvements may be suggested. The inherent flexibility of a microprocessor design should allow enhancements to be incorporated with relative ease.

REFERENCES

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5 A Brief Guide to the Group Terminating Unit — Colin G L Enzer, December 1978

6 Plessey Manual 652/SJ/Ø1243
Section 2. Signalling Format

7 The Matrix Report — J R Paul

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